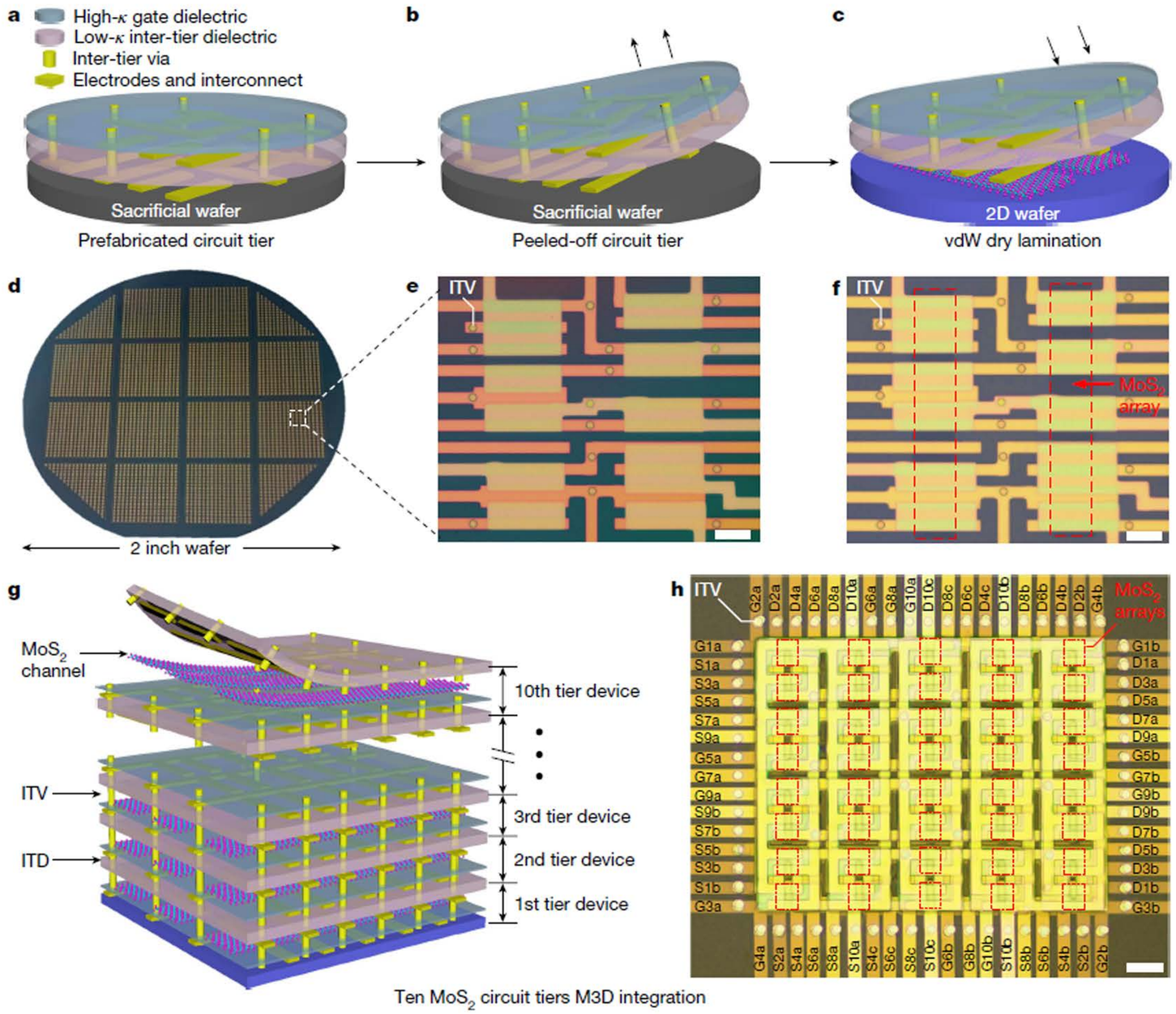
Article

Monolithic three-dimensional tier-by-tier integration via van der Waals lamination

Donglin Lu et al., 2024 April, Nature 630(8016):1-6

展示二維半導體可實現單晶片集成電路堆疊(Monolithic 3D-IC)

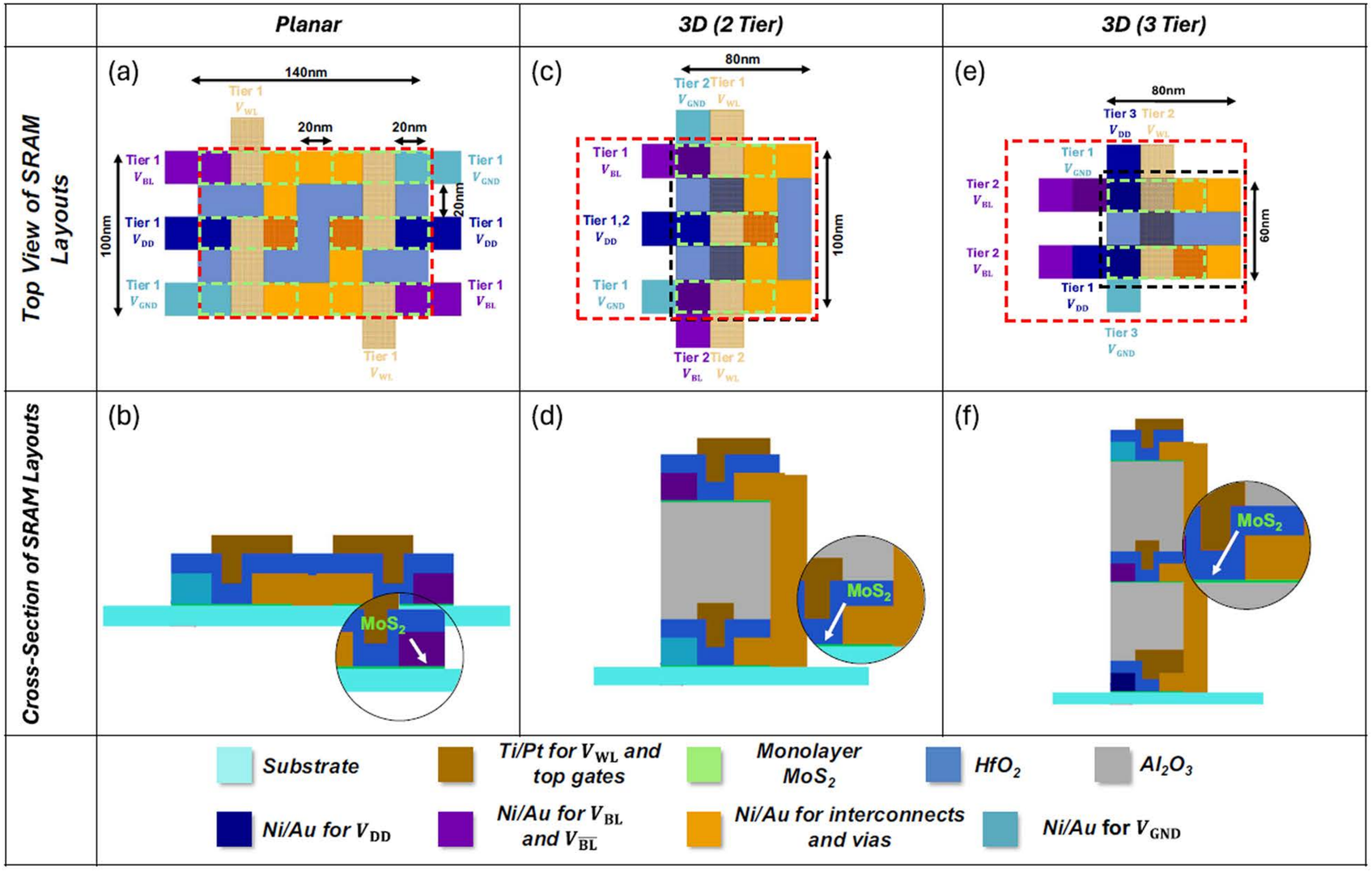


Ten MoS_2 circuit tiers M3D integration

https://doi.org/10.1038/s41467-025-59993-8

Enabling static random-access memory cell scaling with monolithic 3D integration of 2D field-effect transistors

Nature Communications | (2025) 16:4879



首次展示了二維半導體SRAM多層堆疊於CPU層之上，實現延續摩爾定律之潛力