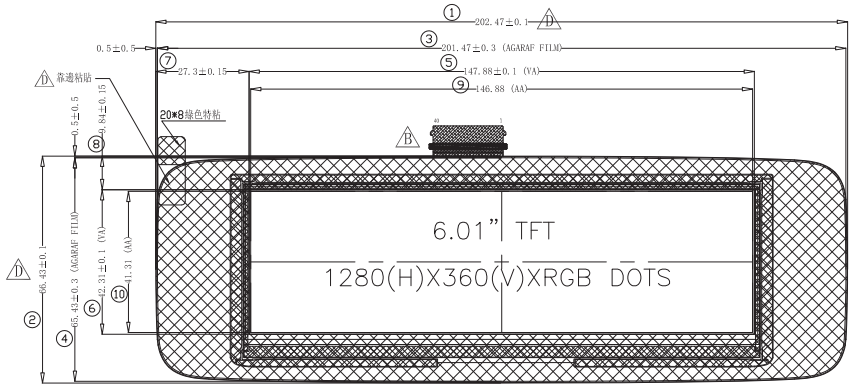

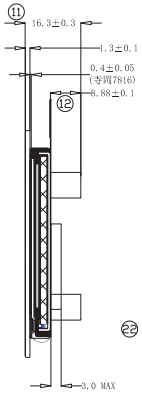

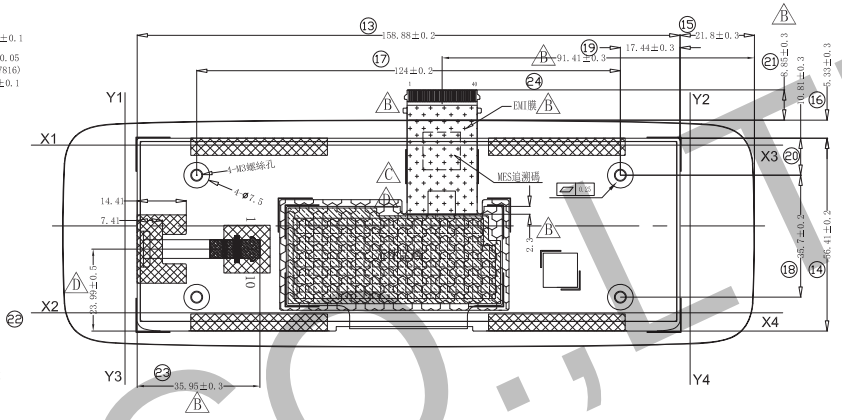

pin	symbol
1	GND
2	GND
3	VCI
4	VCI
5	GND
6	RESET
7	DISP
8	SPI_SDA
9	SPI_SCL
10	SPI_CSX
11	GND
12	GND
13	D3_P
14	D3_N
15	GND
16	CLK_P
17	CLK_N
18	GND
19	D2_P
20	D2_N
21	GND
22	D1_P
23	D1_N
24	GND
25	D0_P
26	D0_N
27	GND
28	FAIL_DET
29	RL
30	TB
31	REST
32	I2C_SCL
33	I2C_SDA
34	EINT
35	GND
36	NC
37	NC
38	NC
39	GND
40	GND

LITEKALL CO.,LTD.

General specification

Item	specifications	Unit
Active screen size	6.0 inch	-
Display resolution	1280x RGB x 360	pixel
Module size (W x H x T)	202.47 × 66.43 × 16.3	mm
Active area (W x H)	146.88 x 41.31	mm
Pixel pitch (W×H)	0.1148 x 0.1148	mm
Interface	LVDS	-
Module weight	TBD±10%	g
Our components and processes are compliant to RoHS standard.		

Item	specifications
LCD type	a-Si TFT
LCD mode	IPS / Normally Black
Polarizer mode	Transmissive
Pixel arrangement	RGB-stripe
Backlight type	LED
Viewing direction(Gray inversion)	85/85/85/85

Interface pin

Pin No.	Symbol	Function
1	GND	Ground pin for logic circuit and I/O (0V).
2	GND	Ground pin for logic circuit and I/O (0V).
3	VCI	Power input for main and I/O power
4	VCI	Power input for main and I/O power
5	GND	Ground pin for logic circuit and I/O (0V).
6	RESET	LCD global reset signal.Active low
7	DISP	Display On:Display mode setting pin.Active high
8	SPI_SDA	Serial Interface address and data input /output for SPI interface
9	SPI_SCL	Serial Interface clock input for SPI interface
10	SPI_CSX	Serial Interface chip enable signal for SPI interface
11	GND	Ground pin for logic circuit and I/O (0V).
12	GND	Ground pin for logic circuit and I/O (0V).
13	D3_P	Data input
14	D3_N	Data input
15	GND	Ground pin for logic circuit and I/O (0V).
16	CLK_P	CLK input
17	CLK_N	CLK input
18	GND	Ground pin for logic circuit and I/O (0V).
19	D2_P	Data input
20	D2_N	Data input
21	GND	Ground pin for logic circuit and I/O (0V).
22	D1_P	Data input
23	D1_N	Data input
24	GND	Ground pin for logic circuit and I/O (0V).
25	D0_P	Data input
26	D0_N	Data input
27	GND	Ground pin for logic circuit and I/O (0V).
28	FAIL_DET	Fail detect signal output.
29	RL	Horizontl shift direction selection for source output.
30	TB	Vertical shift direction selection for gate output.
31	REST(CTP)	TP Extermal reset signal.Active low
32	I2C_SCL(CTP)	TP I2C clock pin
33	I2C_SDA(CTP)	TP I2C data pin
34	EINT(CTP)	TP interrupt pin
35	GND	Ground pin for logic circuit and I/O (0V).
36	NC(BIST)	Not connect(Enable built-in self-test(BIST) function)
37	NC	Not connect
38	NC	Not connect
39	GND	Ground pin for logic circuit and I/O (0V).
40	GND	Ground pin for logic circuit and I/O (0V).