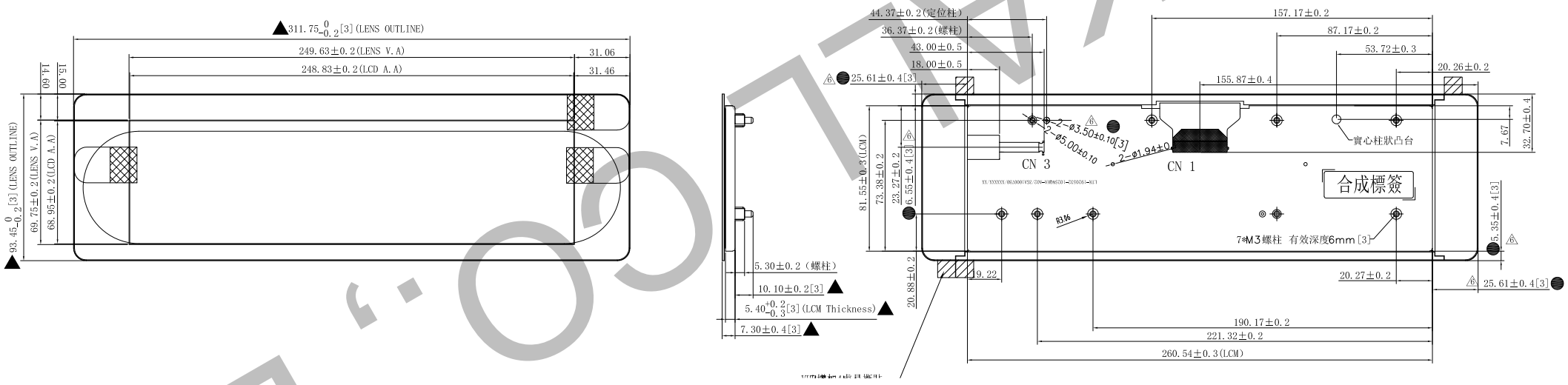

**General specification**

| Item | specifications | Unit |
|---|---|---|
| Active screen size | 10.17 inch Diagonal | - |
| Display resolution | 1920 x (RGB)*3 x 532 | pixel |
| Module size (W x H x T) | 311.75 x 93.45 x7.3 | mm |
| Active area (W x H) | 248.832 x 68.9472 | mm |
| Pixel pitch ( W×H ) | 0.1296 x 0.1296 | mm |
| Interface | LVDS | - |
| Module weight | TBD±10% | g |
| Our components and processes are compliant to RoHS standard. | | |

| Item | specifications |
|---|---|
| LCD type | a-Si TFT |
| LCD mode | IPS / Normal black |
| Polarizer mode | Transmissive |
| Pixel arrangement | RGB-stripe |
| Backlight type | LED |
| Viewing direction(Gray inversion) | 85/85/85/85 |

## Interface pin

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | GND | Ground |
| 2 | PAD_GPM | Gate pulse modulation (GPM) control pin. Normally pull-L.<br>PAD_GPM = “H”: GPM function enabled.<br>Waveforms. PAD_GPM = “L”: Normal operation. (Default) |
| 3 | PAD_LPM2T | 2 CLK long pulse mode select pin. Normally<br>pull-L.PAD_LPM2T =“H”: Long pulse mode.For odd driver<br>outputs: （1）Only odd OEs are activated.<br>（2）GPM function only enabled for even CLK falling period.<br>Start pulse will be limited to 2 CLK if external start pulse<br>more than 2 CLK.<br>PAD_LPM2T = “L”: Single pulse mode. (Default)When<br>PAD_OE= H, all driver outputs are fixed to VEE voltage.<br>Start pulse has no limitation. |
| 4 | PAD_VB | The slew rate control of gate pulse modulation.When<br>PAD_GPM=”H”,the falling slew rate of GPM can be<br>controlled by the connected resistor R.<br>The value of resistor R depends on the loading of gate output. |
| 5 | NC | / |
| 6 | VGL | Power supply for Source and GIA (Require a 2.2uF and<br>0.1uF capacitor to GND as close to FPC as possible.) |
| 7 | NC | / |
| 8 | VGH | Power supply for Source and GIA (Require a 2.2uF and<br>0.1uF capacitor to GND as close to FPC as possible .) |
| 9 | NC | / |
| 10 | VCOM | Internal driving circuit power for LCD common electrode<br>(Require a 2.2uF capacitor to GND as close to FPC as possible )Need to adjust<br>according to the best VCOM of each Panel |
| 11 | NC | Power supply for SD circuit. |
| 12 | VPP | Power input for OTP programming (8.5V).<br>Note1 : Leave this pin open or connect it to VDD when not programming OTP.<br>Note2 : The whole OTP programming procedure sequence<br>(apply 8.5V to VPP pin) should complete in 6 seconds. |
| 13 | NC | / |
| 14~15 | VSP(VDPA) | Power input for source driver and power circuits (Require a<br>10uF capacitor to GND as close to FPC as possible ) |
| 16 | NC | / |
| 17~18 | VSN(VDNA) | Power input for source driver and power circuits (Require a<br>10uF capacitor to GND as close to FPC as possible ) |
| 19 | NC | / |
| 20 | VDDN1 | Internal regulator out for negative level shifter(-3.6v),(Require a 2.2uF capacitor to<br>GND as close to FPC as possible when PCBA design) |
| 21 | I2C_SCL | Serial communication clock pin for I2C interface External<br>pull high resistor, 4.7 KΩ, is needed. |
| 22 | I2C_SDA | Serial Interface address and data input/output for I2C<br>interface.External pull high resistor, 4.7 KΩ, is needed. |
| 23~27 | NC | / |
| 28 | VDD | Power input for main and I/O power |
| 29 | DVDD | Internal regulator output for logic power supply |
| 30 | DVDD_IF | Internal regulator output for interface power supply |
| 31 | GND | Ground. |

| Pin No. | Symbol | Function |
|---|---|---|
| 32 | OLV3P | LVDS data lane 3 Positive |
| 33 | OLV3N | LVDS data lane 3 Negative |
| 34 | GND | Ground. |
| 35 | OLVCLKP | LVDS Clock Lane Positive |
| 36 | OLVCLKN | LVDS Clock Lane Negative |
| 37 | GND | Ground. |
| 38 | OLV2P | LVDS data lane 2 Positive |
| 39 | OLV2N | LVDS data lane 2 Negative |
| 40 | GND | Ground. |
| 41 | OLV1P | LVDS data lane 1 Positive |
| 42 | OLV1N | LVDS data lane 1 Negative |
| 43 | GND | Ground. |
| 44 | OLV0P | LVDS data lane 0 Positive |
| 45 | OLV0N | LVDS data lane 0 Negative |
| 46 | GND | Ground. |
| 47 | VGMPHI | Internal regulator output for positive gamma reference voltage (Require a 2.2uF capacitor to GND as close to FPC as possible ) |
| 48 | VGMPLI | Internal regulator output for positive gamma reference voltage (Require a 2.3uF capacitor to GND as close to FPC as possible ) |
| 49 | VGMNHI | Internal regulator output for positive gamma reference voltage (Require a 2.4uF capacitor to GND as close to FPC as possible ) |
| 50 | VGMNLI | Internal regulator output for positive gamma reference voltage (Require a 2.5uF capacitor to GND as close to FPC as possible ) |
| 51 | ERROPB | For ASIL detection results output.<br>ERROPB = 1, abnormal.<br>ERROPB = 0, normal.<br>(Please reserve a test point when PCBA design) |
| 52 | STBYB | Standby mode.<br>STBYB = 1, normal operation.<br>STBYB = 0, timing controller and source driver will turn offand all output are 0V. |
| 53 | GRB | Global reset pin GRB = 1, normal operation.<br>GRB = 0, the driver is in reset state.<br>Suggest to connect with an RC reset circuit for stability |
| 54 | UPDN | For Up or Down sequence control.<br>UPDN = 1, U2D sequence<br>UPDN = 0, D2U sequence |
| 55 | SHLR | Source Right or Left sequence control.<br>SHLR= 0, shift left: last data = S0←S1←S2.....← S1922= first data.<br>SHLR= 1, shift right: first data = S0→S1→S2.....→S1922= last data. |
| 56~57 | NC | / |
| 58 | BIST | Normal Operation/BIST pattern select.<br>BIST = 1, BIST mode. (CLK input is not needed)<br>BIST = 0, normal operation. |
| 59 | VCOM | Internal driving circuit power for LCD common electrode (Require a 2.2uF capacitor to GND as close to FPC aspossible )Need to adjust according to the best VCOM of each Panel |
| 60 | GND | Ground. |