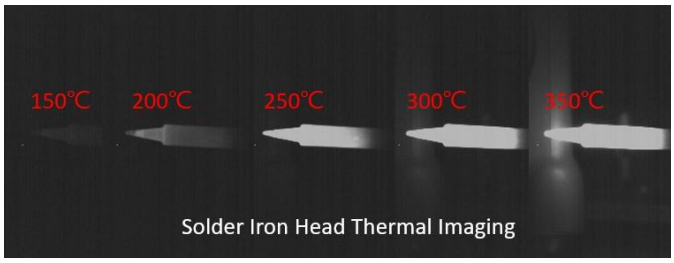
Near-Infrared (0.9 – 1.7μm) 320x256 InGaAs Focal Plane Array

FEATURES

- 320x256 Array Format
- 0.9μm – 1.7μm Spectral Range
- Light Weight 44CLCC Package
- Minimum Pixel Operability > 99.9%
- Quantum Efficiency > 70%
- Room Temperature Operation
- Built-in Temperature Sensor
- Snapshot ITR/IWR and IMRO Readout Modes
- 1, 2 or 4 Outputs with up to 10 MHz Pixel Rate
- Windowing Capability

APPLICATIONS

- Near-Infrared Imaging
- Covert Surveillance
- Semiconductor/Solar Panel Inspection
- Medical Science and Biology
- Fiberoptic Assembly and Testing
- See through Fog/Smoke
- Ice/Slush/Moisture Mapping
- Industrial Thermal Imaging
- Astronomy and Scientific
- Sorting Recycling



High GAIN mode with 10 ms integration time

GENERAL DESCRIPTIONS

PARAMETER	UNIT	VALUE
Sensor Technology	---	Planar InGaAs PIN
Spectral Range	μm	0.9 – 1.7
Actual Pixel Array	---	320 x 256
Effective Pixel Array	---	318 x 254
Pixel Pitch	μm	30
Image Size	mm	9.6 x 7.68
Package Type	---	44-pin Ceramic LCC
Package Size L x W x T	mm	16.510 x 16.510 x 2.456
Weight	g	1.6

For further information, please visit our website at www.clpt.com.tw or contact us via sales@clpt.com.tw

SPECIFICATIONS (T_{AMB} = 22℃)

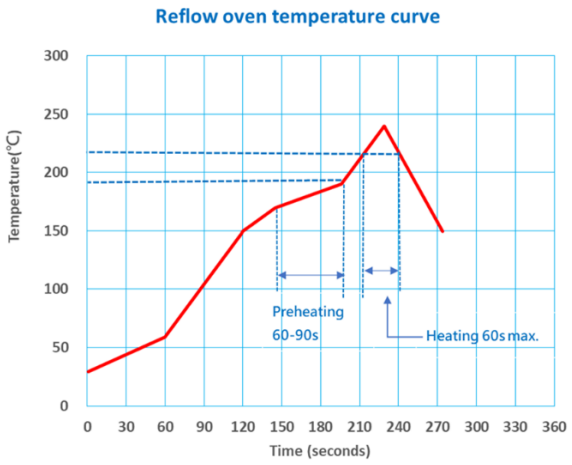
Parameter		Unit	Typical Value	Conditions
[1.2]Dark Current		fA	≤ 200	Photopixel Biased @ -0.5 V
[1.2]Quantum Efficiency * Fill Factor (QEFF)		%	≥ 70	λ = 1.0 µm – 1.6 µm
[1.2]Response Nonuniformity		%	≤ 10	At 50% Full Well
[1.2]Response Nonlinearity		%	≤ 2	15% – 85% Well Occupation Range
[2]Charge Capacity	@High Gain, 13.3 µV/e⁻	Me⁻	0.17	ROIC Specifications
	@Low Gain, 0.7 µV/e⁻		3.50	
Readout Noise		e⁻RMS	≤ 70	ROIC Specifications High Gain, Tint = 16msec
Output Swing		V	2.8	
[2]Minimum Integration Period		µs	5.5	Assuming 5MHz Master Clock
[1.2]Pixel Operability		%	Min. Value	Percentage of Pixels with QEFF
			≥ 99.9	Deviation within ± 20%*(QEFF Mean)

1. These items are defined for central effective pixel array (318x254). Their values correspond to default operation conditions.
2. Contact us for further information.

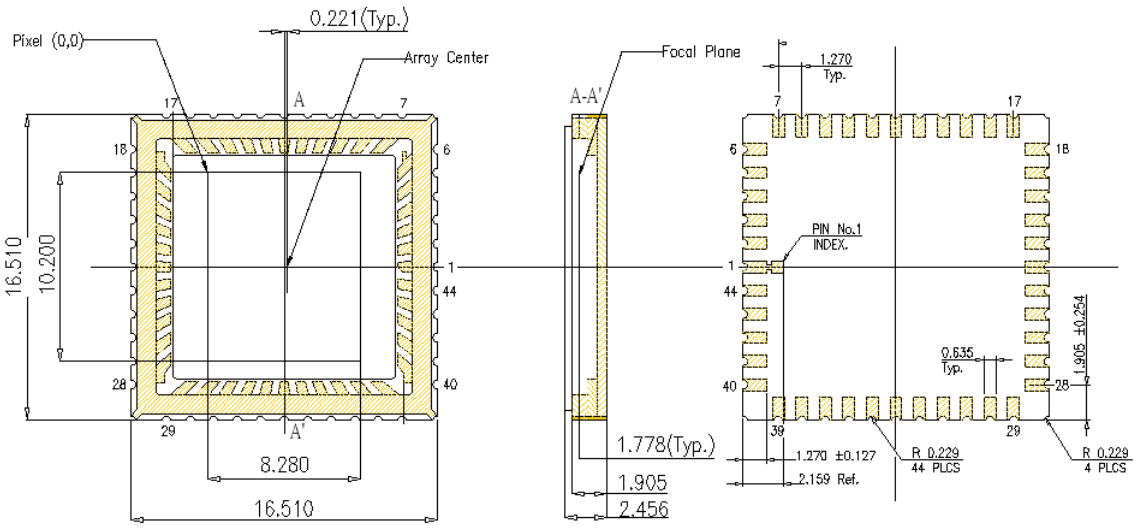
ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Min.	Max.
[3]Operating Temperature	℃	-40	+71
[3]Storage Temperature	℃	-40	+71
Power Consumption	mW	---	175
Reflow Condition	℃	---	≦240℃ (within 60 sec)

3. In non-condensing environment



PACKAGE OUTLINE (Unit: mm)



PIN DEFINITION							
01	GAIN	12	NC	23	VPOSOUT	34	NC
02	DATA	13	NC	24	VOS	35	NC
03	FSYNC	14	NC	25	VBLM	36	NC
04	LSYNC	15	NC	26	VOUTREF	37	NC
05	CLK	16	NC	27	VCAS	38	NC
06	VPD	17	VNEGOUT	28	IMSTR_ADJ	39	VDETCOM
07	VND	18	OUTA	29	VNEG	40	VPOS_CORE
08	NC	19	OUTB	30	VPOS	41	TEMP
09	NC	20	OUTC	31	NC	42	TESTOUT
10	NC	21	OUTD	32	NC	43	VTESTIN
11	NC	22	OUTR	33	NC	44	BWL

OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
06	VPD	5.5V	< 1mA	Logic positive supply
07	VND	0V	< 1mA	Logic negative supply
23	VPOSOUT	5.5V	< 25mA	Output stage analog supply
17	VNEGOUT	0V	< 25mA	Output stage analog ground
30	VPOS	5.5V	< 5mA	Positive analog supply
29	VNEG	0V	< 15mA	Negative analog supply and substrate
40	VPOS_CORE	5.5V	< 15mA	CTIA amplifier positive supply
39	VDETCOM	4.7V – 5.5V	< 5mA	Detector common voltage [4]Detector bias = VDETCOM-4.7

4. VDETCOM lower than 4.7V will forward bias the sensor, the exact zero bias voltage is device and temperature dependent.

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
05	CLK	0V – 5.5V	< 10ns	Master clock Max. Freq.=5MHz
03	FSYNC	0V – 5.5V	< 10ns	Frame sync – controls frame start and integration time
04	LSYNC	0V – 5.5V	< 10ns	Line sync – controls line readout timing
02	DATA	0V – 5.5V	< 10ns	Data code input – programs device function registers in Control Mode Left open in Default Mode

Clocks	Synchronization
FSYNC	Rising and falling when CLK is rising
LSYNC	Rising and falling when CLK is falling
DATA	Rising and falling when CLK is rising

Analog Video Output

Pin #	Outputs	Levels	Settle	Remark
18	OUTA	1.3V to 4.2V	< 50ns to 0.1%	Output A used in single output mode
19	OUTB	1.3V to 4.2V	< 50ns to 0.1%	Output A and B used in two output mode
20	OUTC	1.3V to 4.2V	< 50ns to 0.1%	Output A, B, C, and D used in four output mode
21	OUTD	1.3V to 4.2V	< 50ns to 0.1%	Output A, B, C, and D used in four output mode
22	OUTR	3V	---	Reference for common mode output

Gain & Bandwidth Selection in Default Mode

Pin #	Functions	Low	High	Remark
01	GAIN	0V C=10fF	5.5V C=210fF	Selects unit cell integration capacitor Left open in Control Mode
44	BWL	0V Low BW	5.5V High BW	Selects bandwidth limiting capacitor in unit cell Left open in Control Mode

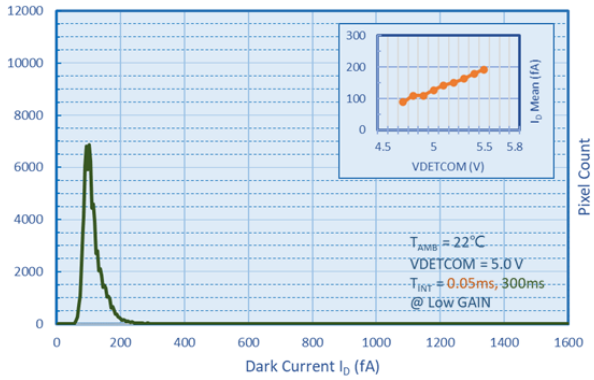
Advanced Function

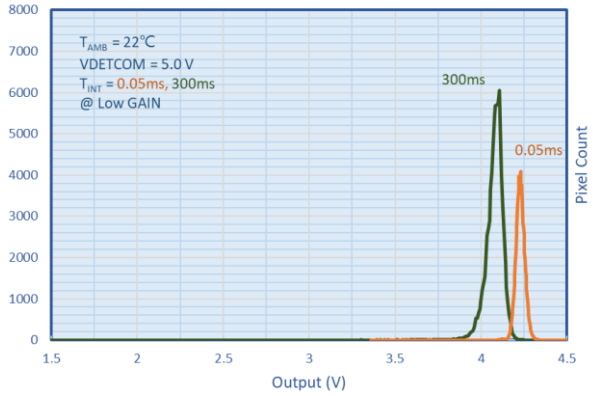
Pin #	Functions	Voltages	Remark
27	[5]VCAS	3.75V	CTIA amplifier cascode FET bias
26	[5]VOUTREF	3V	Output reference level during blanking period
25	[5]VBLM	2V	Detector bloom control
28	[6]IMSTR_ADJ	0V – 5.5V	Adjusts analog master bias current
24	VOS	0V – 5.5V	Variable Offset/Skimming Control Voltage
41	TEMP	0V – 5.5V	On chip temperature monitor 0.74V at 300K, Slope=-14.8mV/10K in 50 – 300K
43	VTESTIN	1.5V – 4.5V	For use in IC function test
42	TESTOUT	0V – 5.5V	Left open in FPA operation

5. Internally generated after bias input, but can be overridden.
6. Also addressable through control register (DATA).

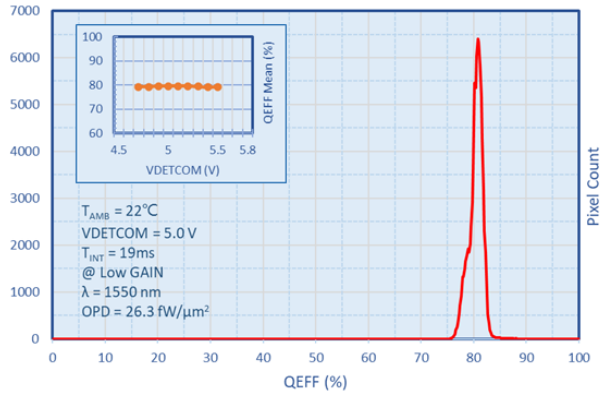
EXAMPLE CURVES

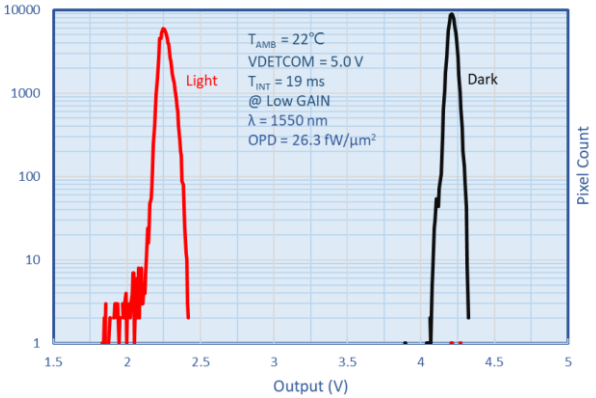
Histograms of Dark Condition



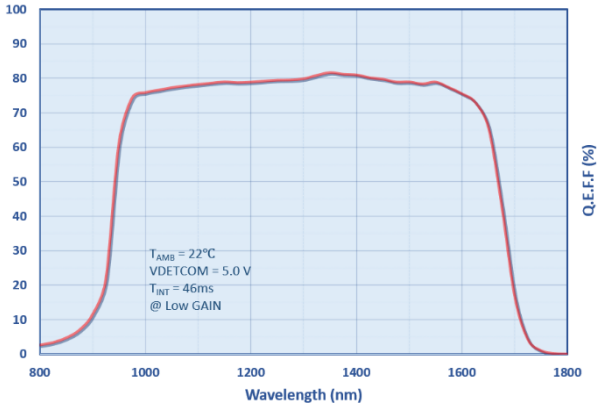


Histograms of Illumination Condition

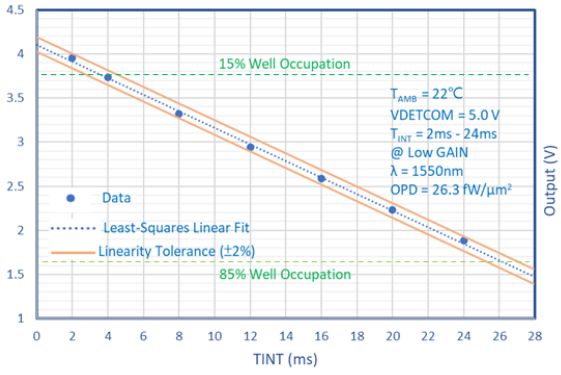




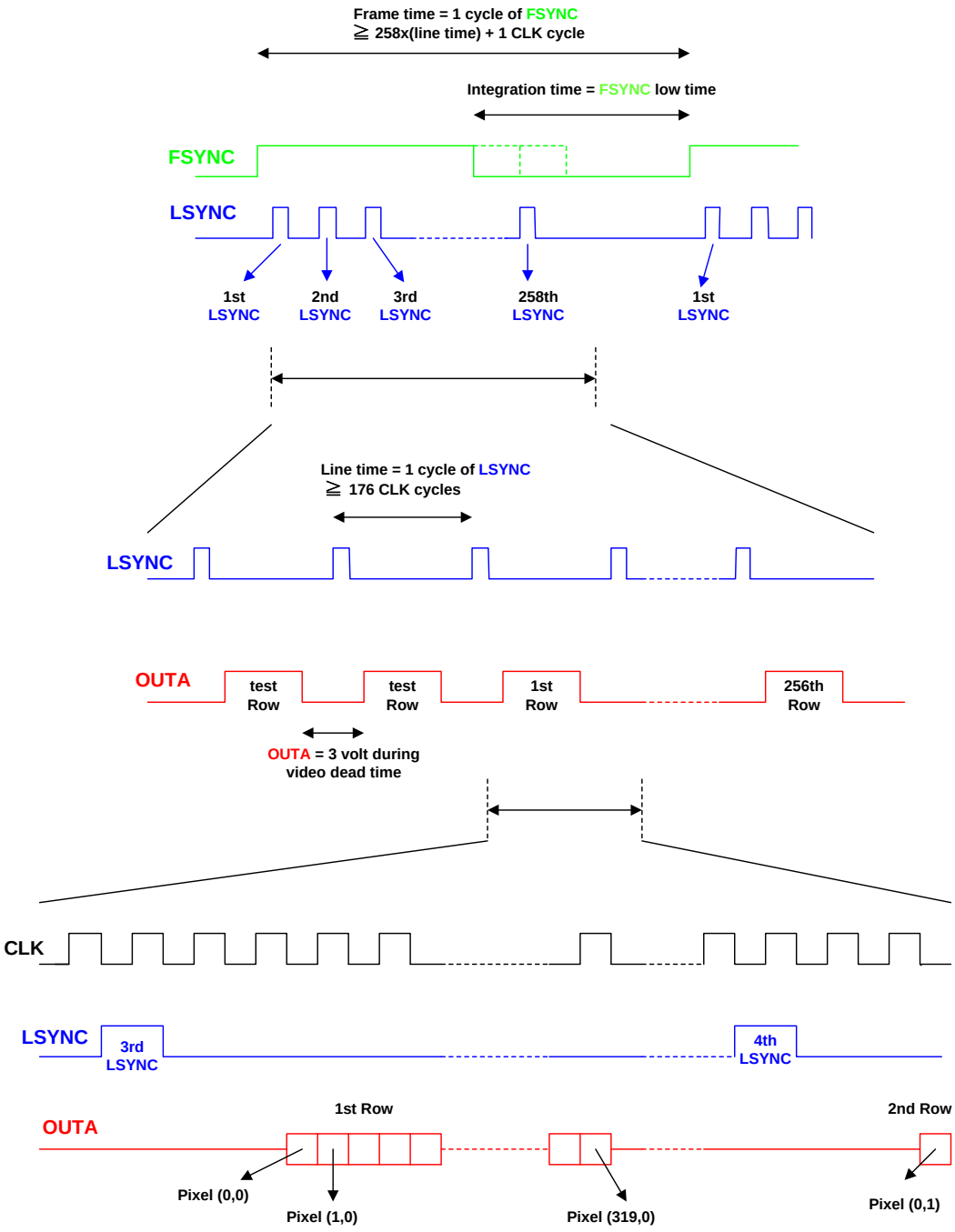
QEFF Spectrum



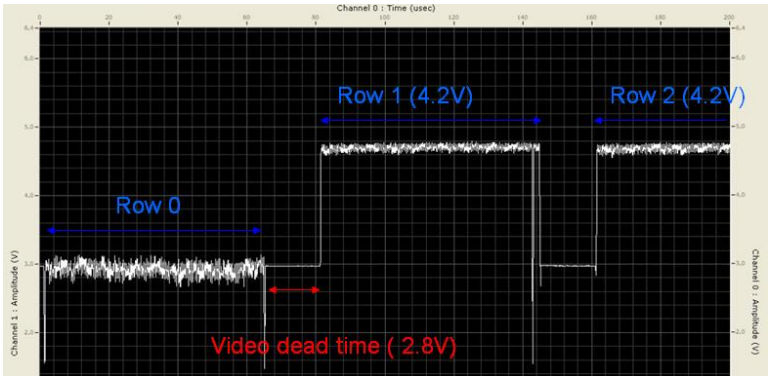
Output Linearity



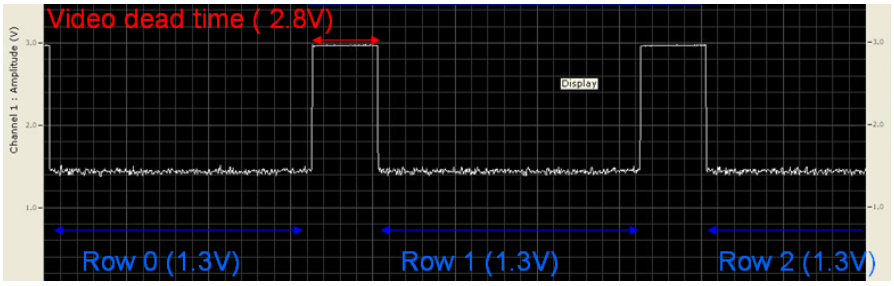
TIMING CHART FOR DEFAULT MODE OPERATION



OUTA waveform under dark



OUTA waveform under saturation



OUTA waveform under half saturation