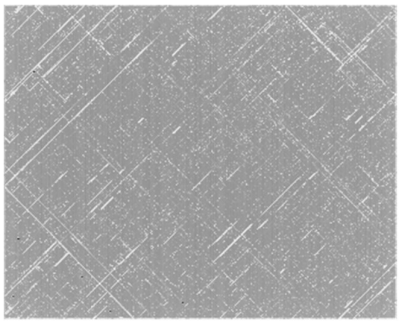
Near-Infrared (1.2 – 2.2µm) 320x256 InGaAs Focal Plane Array

FEATURES

- 320x256 Array Format
- 28-pin Metal DIP Package
- Embedded Thermoelectric Cooler
- Built-in Temperature Sensor
- 1.2µm – 2.2µm Spectral Range
- Minimum Pixel Operability > 98%
- Quantum Efficiency > 65%
- Snapshot ITR / IWR and IMRO Readout Modes
- 1, 2 or 4 Outputs with up to 10 MHz Pixel Rate
- Windowing Capability

APPLICATIONS

- Shortwave-Infrared Imaging
- Hyper- / Multi-Spectral Imaging
- Semiconductor Inspection / Process Monitoring
- Medical Science and Biology
- Fiberoptic Assembly and Testing
- See through Fog / Smoke
- Ice / Slush / Moisture Mapping
- Laser Beam Profiling
- Astronomy and Scientific
- Sorting Recycling



Raw Image @ -40°C

GENERAL DESCRIPTIONS

PARAMETER	UNIT	VALUE
Sensor Technology	---	Planar InGaAs PIN
Spectral Range	µm	1.2 – 2.2
Actual Pixel Array	---	320 x 256
Effective Pixel Array	---	318 x 254
Pixel Pitch	µm	30
Image Size	mm	9.6 x 7.68

For further information, please visit our website at www.clpt.com.tw or contact us via sales@clpt.com.tw

Package Type	---	28-pin Metal DIP Package
Package Size L x W x T	mm	50.0 x 25.4 x 11.67
Weight	g	24.0

SPECIFICATIONS ([1]ITS = -40℃)

Parameter		Unit	Typical Value	Conditions
[2.3]Dark Current		pA	10	Photopixel Biased @ 0 V
[2]Quantum Efficiency * Fill Factor (QEFF)		%	≥ 65	λ = 1700 nm
[2]Response Nonuniformity		%	≤ 10	At 50% Full Well
[2]Response Nonlinearity		%	≤ 10	15% – 85% Well Occupation Range
Charge Capacity	@High Gain, 13.3 μV/e^-	Me^-	0.17	ROIC Specifications
	@Low Gain, 0.7 μV/e^-		3.50	
Readout Noise		e^-_{RMS}	≤ 70	ROIC Specifications
Output Swing		V	2.7	
Minimum Integration Period		μs	5.5	Assuming 5MHz Master Clock
[2]Pixel Operability		%	Min. Value	Percentage of Pixels with QEFF
			≥ 98	Deviation within ± 45%*(QEFF Mean)

1. Readings from Integrated Temperature Sensor (ITS).
2. These items are defined for central effective pixel array (318x254). Their values correspond to default operation conditions.
3. Low Gain, Tint = 4ms –0.01ms.

ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Min.	Max.
[4]Operating Temperature	℃	-40	+71
[4]Storage Temperature	℃	-40	+71
[5]Power Consumption	mW	---	175

4. In non-condensing environment.
5. Without powering on the thermoelectric cooler.

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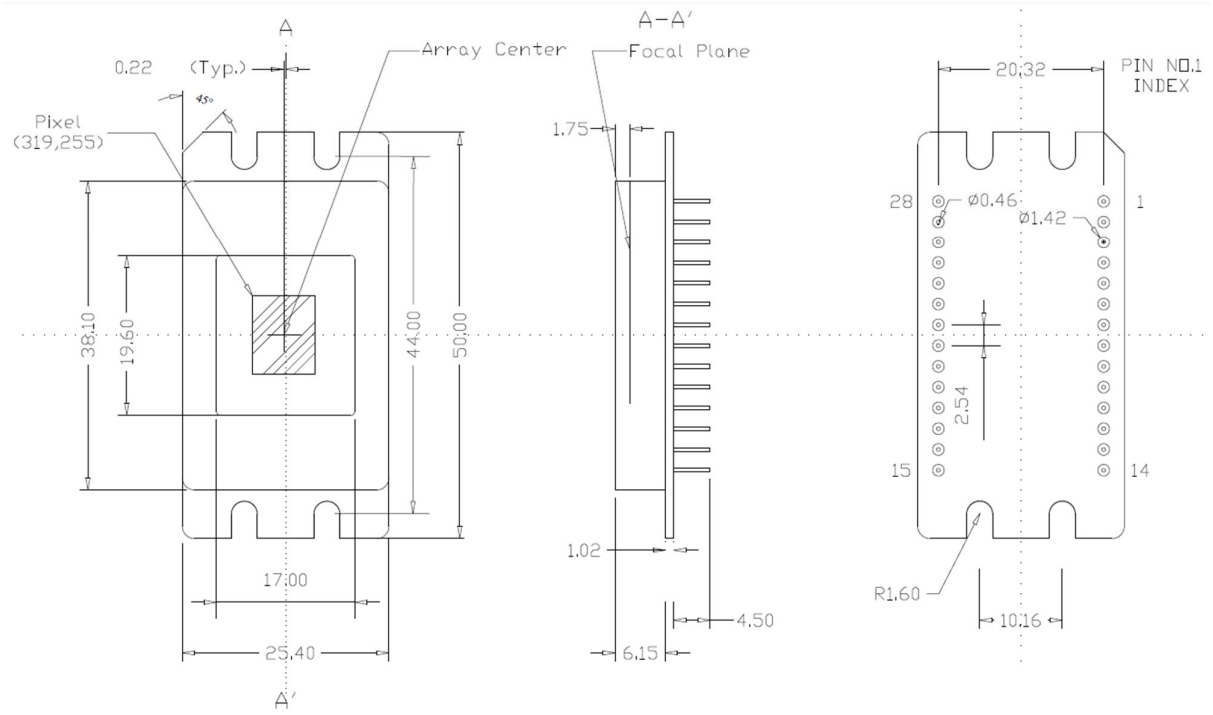
PACKAGE OUTLINE (Unit: mm)



PIN DEFINITION							
01	VPOS	08	DATA	15	VNEGOUT	22	VOS
02	VDETCOM	09	FSYNC	16	OUTA	23	VBLM
03	TEC+	10	LSYNC	17	OUTB	24	VOUTREF
04	VPOS_CORE	11	CLK	18	OUTC	25	VCAS
05	TEMP	12	VPD	19	OUTD	26	TEC-
06	BWL	13	VND	20	OUTR	27	IMSTR ADJ
07	GAIN	14	CASE GROUND	21	VPOSOUT	28	VNEG

OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
12	VPD	5.5V	< 1mA	Logic positive supply
13	VND	0V	< 1mA	Logic negative supply
21	VPOSOUT	5.5V	< 25mA	Output stage analog supply
15	VNEGOUT	0V	< 25mA	Output stage analog ground
01	VPOS	5.5V	< 5mA	Positive analog supply
28	VNEG	0V	< 15mA	Negative analog supply and substrate
04	VPOS_CORE	5.5V	< 15mA	CTIA amplifier positive supply
02	VDETCOM	4.5V – 5.0V	< 5mA	Detector common voltage Detector bias = VDETCOM-4.5

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
11	CLK	0V – 5.5V	< 10ns	Master clock Max. Freq.=5MHz
09	FSYNC	0V – 5.5V	< 10ns	Frame sync – controls frame start and integration time
10	LSYNC	0V – 5.5V	< 10ns	Line sync – controls line readout timing
08	DATA	0V – 5.5V	< 10ns	Data code input – programs device function registers in Control Mode Left open in Default Mode

Clocks	Synchronization
FSYNC	Rising and falling when CLK is rising
LSYNC	Rising and falling when CLK is falling
DATA	Rising and falling when CLK is rising

Analog Video Output

Pin #	Outputs	Levels	Settle	Remark
16	OUTA	1.3V to 4.2V	< 50ns to 0.1%	Output A used in single output mode
17	OUTB	1.3V to 4.2V	< 50ns to 0.1%	Output A and B used in two output mode
18	OUTC	1.3V to 4.2V	< 50ns to 0.1%	Output A, B, C, and D used in four output mode
19	OUTD	1.3V to 4.2V	< 50ns to 0.1%	Output A, B, C, and D used in four output mode
20	OUTR	3V	---	Reference for common mode output

Gain & Bandwidth Selection in Default Mode

Pin #	Functions	Low	High	Remark
07	GAIN	0V C=10fF	5.5V C=210fF	Selects unit cell integration capacitor Left open in Control Mode
06	BWL	0V Low BW	5.5V High BW	Selects bandwidth limiting capacitor in unit cell Left open in Control Mode

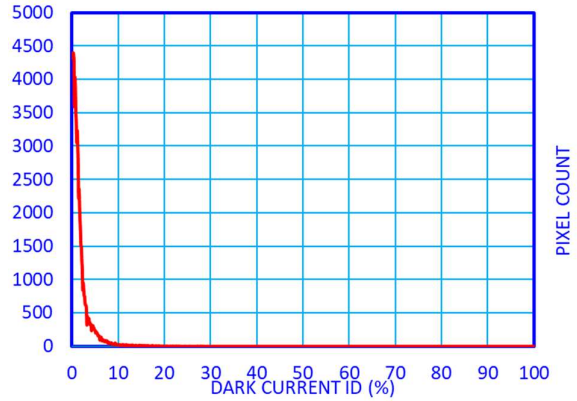
Advanced Function

Pin #	Functions	Voltages	Remark
25	[7]VCAS	3.75V	CTIA amplifier cascode FET bias
24	[7]VOUTREF	3V	Output reference level during blanking period
23	[7]VBLM	2V	Detector bloom control
27	[8]IMSTR_ADJ	0V – 5.5V	Adjusts analog master bias current
22	VOS	0V – 5.5V	Variable Offset/Skimming Control Voltage
05	TEMP	0V – 5.5V	On chip temperature monitor 0.74V at 300K, Slope=-14.8mV/10K in 50 – 300K

6. Internally generated after bias input, but can be overridden.
7. Also addressable through control register (DATA).

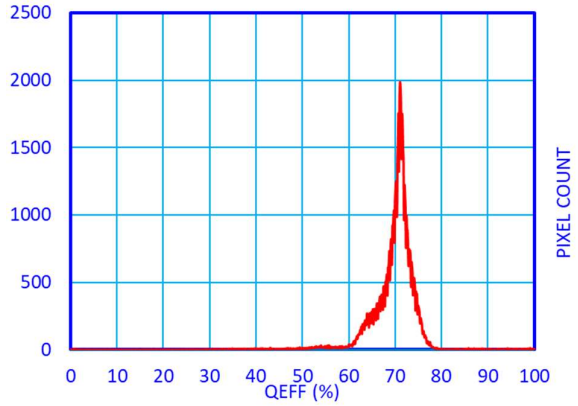
EXAMPLE CURVES

Histograms of Dark Condition



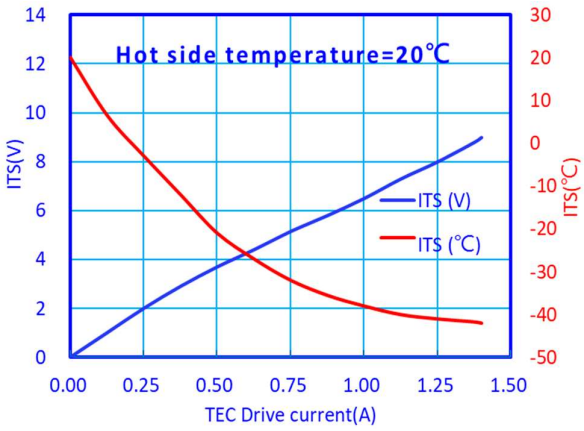
Measurement Conditions	
Illumination	Dark
Gain	Low
Integration Time	4.5 ms
ITS	-40˚C
Detector Bias	Vdetcom = 4.5 V
Outputs	OUTA, 1 output mode
Screen Size	318 x 254

Histograms of Illumination Condition

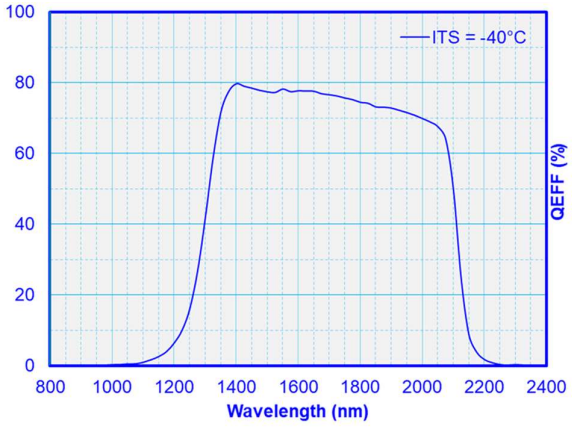


Measurement Conditions	
Illumination	1700 nm
Gain	Low
Integration Time	3.5 ms
ITS	-40˚C
Detector Bias	Vdetcom = 4.5 V
Outputs	OUTA, 1 output mode
Screen Size	318 x 254

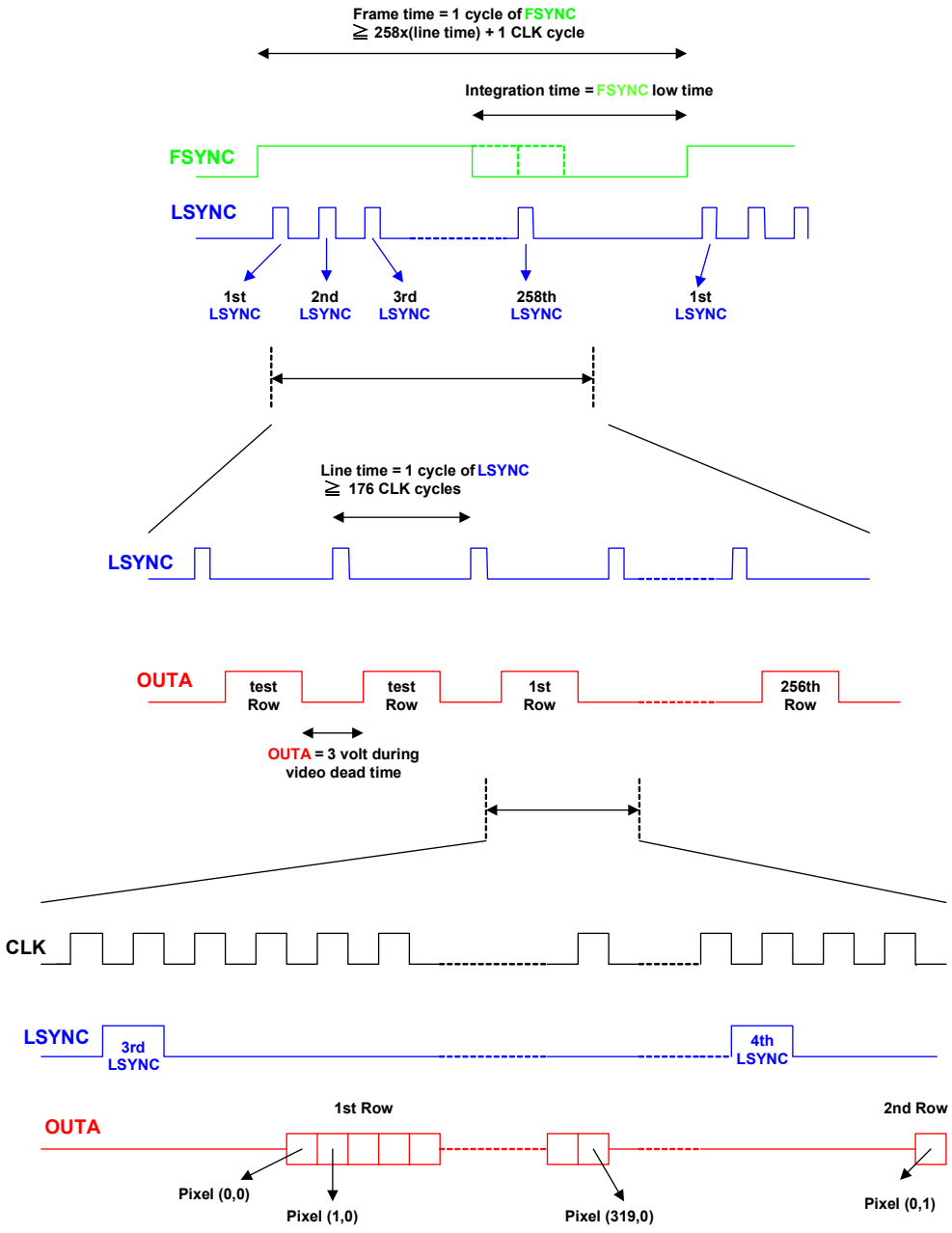
Cooling Performance



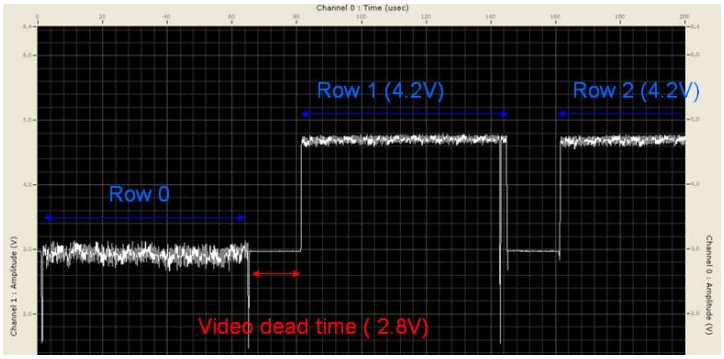
QEFF Spectrum



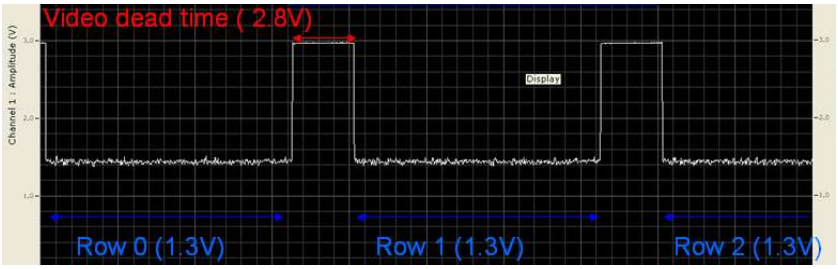
TIMING CHART FOR DEFAULT MODE OPERATION



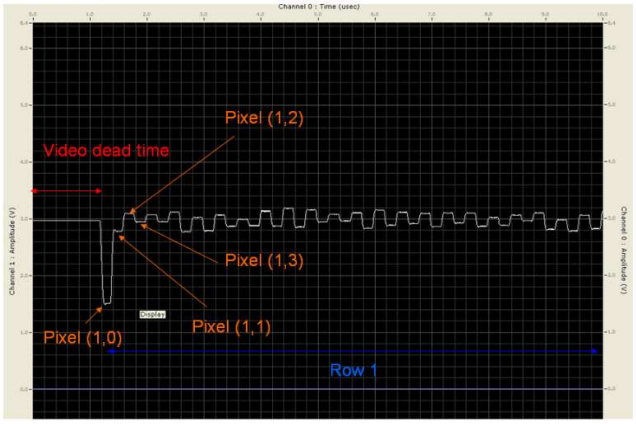
OUTA waveform under dark



OUTA waveform under saturation



OUTA waveform under half saturation



THERMOELECTRIC COOLER DATA (Without thermal loading)

△Tmax	Imax	Vmax
91℃	2.4A	6.4V